I CLAIM:

1. A physically non-distributed microprocessor-based computer system, comprising:

a microprocessor;

a random access memory device;

a mass storage device;

an input-output port device;

said devices each being operable in conjunction with said microprocessor and including an interface for receiving and transmitting data in packet form; and

a packet-based data channel extending between said microprocessor and said interfaces of said devices for providing simultaneous bi-directional communication between said microprocessor and said devices.

2. A computer system as defined in claim 1 wherein said data channel comprises a first signal path in one direction and a second signal path in the other direction.

3. A computer system as defined in claim 1 wherein said data channel includes switching means for selectively connecting said microprocessor to selected ones of said devices.

4. A computer as defined in claim 3 wherein said

30

switching means comprise a microprocessor controlled switch
providing individual interconnection between said microprocessor
and any one of said devices or between any two or more of said
devices.

5

     5.   A computer as defined in claim 3 wherein said
switching means comprises a ring circuit connecting each of said
interface circuits.

10

     6.   A computer as defined in claim 1 wherein said
packets include a request-type packet and a reply-type packet,
said reply packet being sent by said devices in reply to receipt
of said request packet by said device.

15

     7.   A computer as defined in claim 6 wherein said
request packet includes indicia indicating the size of the reply
packet to be returned.

     8.   A computer as defined in claim 7 wherein each of
20   said data packets includes a header, and said header includes
data indicative of the size of the expected reply packet.

     9.   A computer as defined in claim 7 wherein the size
of the reply packet to be sent is dependent on the plurality of

prior such transactions, where such said transactions result from similar requests for packets of data.

10.   A computer system as defined in claim 1 wherein said interface circuits each include a means whereby the data transmitted from the associated device in a packet remains in storage pending receipt of a reply packet.

11.   A computer system as defined in claim 1 wherein said packets include inquiry-type packets reply-type packets, and idle-type packets.

12.   A computer system as define d in claim 11 wherein said idle-type packets are periodically sent when one of said devices is not requesting an action from any other said devices or responding to an action from any other said devices.

13.   A computer system as defined in claim 1 wherein said interface circuits each include:

a linc cache;

said linc cache being organized with a variable line size direct mapped cache; and

said cache line is larger than the cache line in the host cache.